7250
COIL PRE-DRIVER FOR BUBBLE MEMORIES

Features

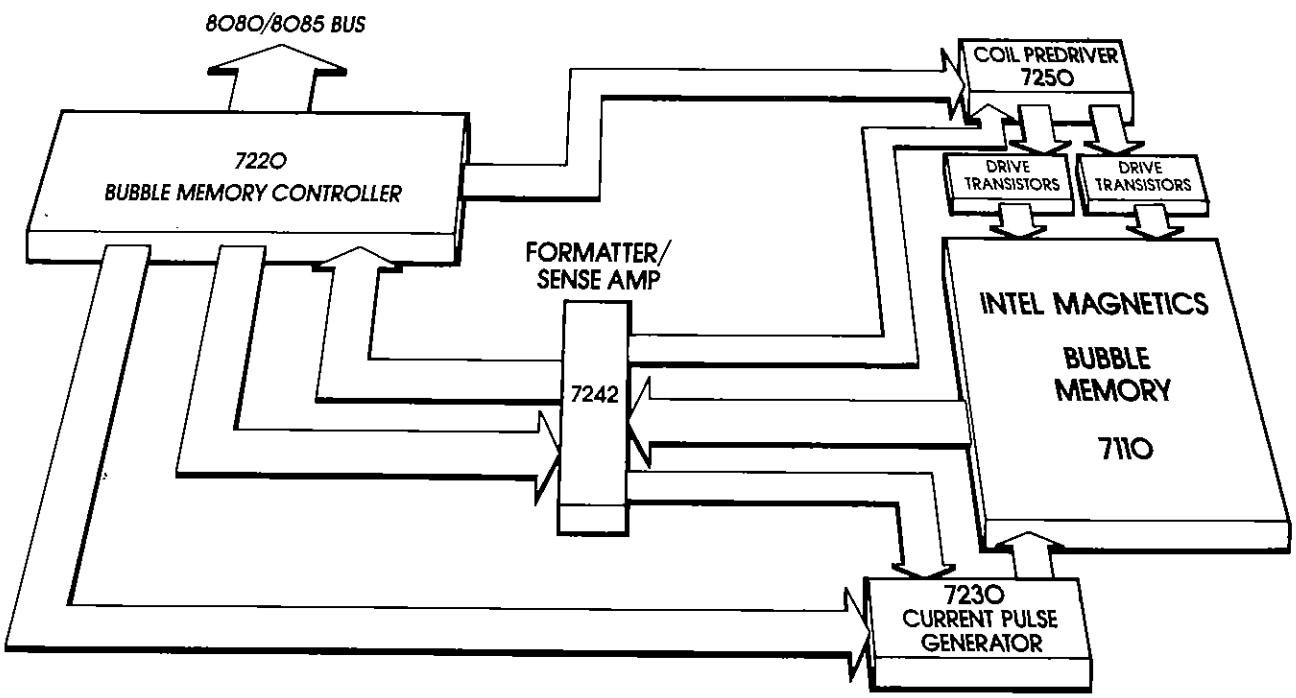
- Ideal for Use with IM's Bubble Memories
- Very Low Power
- Power Fail Reset for Maximum Protection of Bubble Memory
- TTL Compatible Inputs
- Only One Power Supply Required, +12V
- CMOS Technology
- Standard 16-Pin Dual In-Line Package

Description

The Intel 7250 is a low power Coil Pre-Driver (CPD) for use with Intel Magnetics Bubble Memories. The 7250 is controlled by the Intel 7220 Bubble Memory Controller (BMC) and directly drives either Quad VMOS transistor packs or Quad Bipolar transistor packs which are connected to the coils of the bubble memory.

The 7250 is a high voltage, high current driver constructed using CMOS technology. The device has TTL compatible inputs and the outputs are designed to drive either low on-resistance VMOS transistors or bipolar transistors.

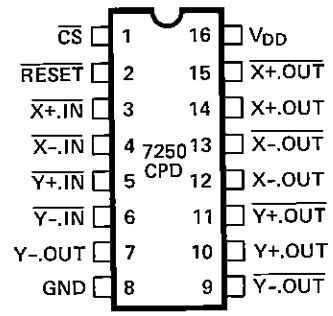
The 7250 is in a standard 16-pin dual in-line package.



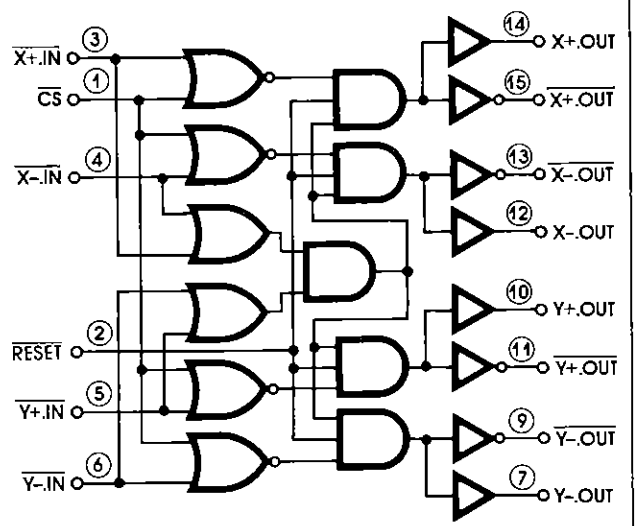
Block Diagram of Single Bubble Memory System — 128K Bytes

7250

Pin Configuration



Logic Diagram



Pin Description

$\overline{CS}$ (Pin 1)

Chip select. It is active low. When high chip is deselected and I_{DD} is significantly reduced.

$\overline{RESET}$ (Pin 2)

Active low input from $\overline{RESET.OUT}$ of 7220 Controller results in removal of power from the chip so that bubble memory is protected in the event of power supply failure.

$\overline{X+.IN}$, $\overline{X-.IN}$ (Pins 3, 4)

Active low inputs from controller which turn on the high current X outputs.

X−.OUT, $\overline{X-.OUT}$, $\overline{X+.OUT}$, X+.OUT (Pins 12-15)

High current outputs and their complements for driving the gates of the 7254 VMOS quad transistors which in turn drive the X coils of the bubble memory.

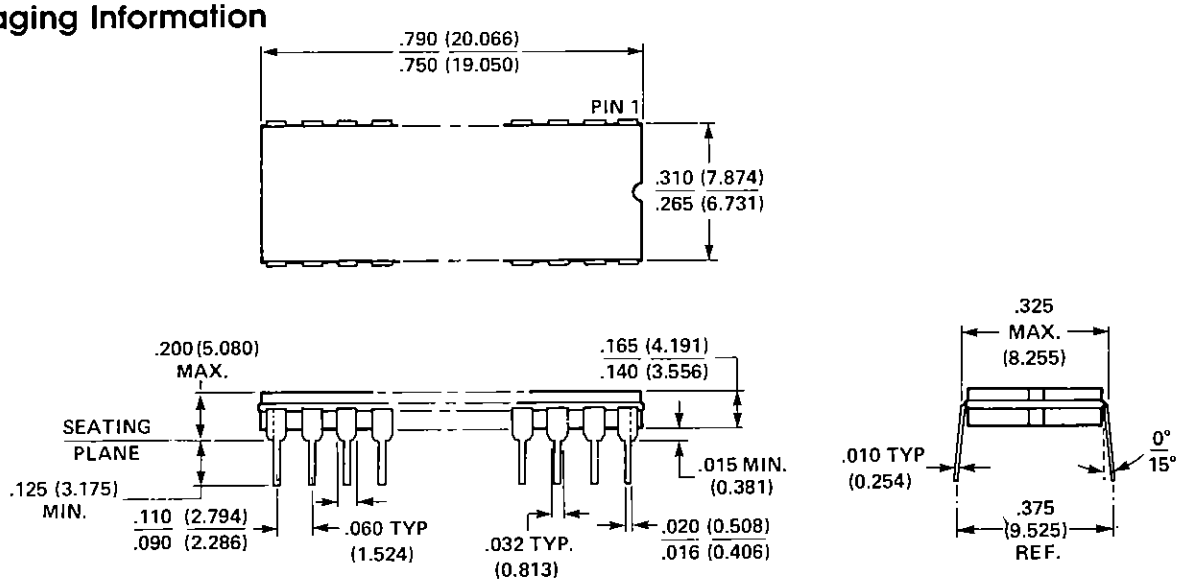
$\overline{Y+.IN}$, $\overline{Y-.IN}$ (Pins 5, 6)

Active low inputs from controller which turn on the high current Y outputs.

$\overline{Y-.OUT}$, Y+.OUT, $\overline{Y+.OUT}$, Y−.OUT (Pins 9-11 and 7)

High current outputs and their complements for driving the gates of the 7254 VMOS quad transistors which in turn drive the Y coils of the bubble memory.

Packaging Information



16-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD}=12V ± 5%, unless otherwise specified

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
$\|I_{IN}\|$	Input Current			10	µA	V_I=0.8V
V_{IL}	Low Level Input Voltage			0.8	V	
V_{IH}	High Level Input Voltage	2.2			V	
V_{OL1}	Output Low Voltage			2.0	V	I_{OL}=200mA
V_{OL2}	Output Low Voltage			0.2	V	I_{OL}=10mA
V_{OH1}	Output High Voltage	V_{DD}-2			V	I_{OH}=-200mA
V_{OH2}	Output High Voltage	V_{DD}-0.2			V	I_{OH}=-10mA
I_{OL}	Output Sink Current	200			mA	V_{OL}=2.0V, 30% Duty Cycle
$\|I_{OH}\|$	Output Source Current	200			mA	V_{OH}=V_{DD}-2.0V, 30% Duty Cycle
I_{DD0}	Supply Current			4.5	mA	Chip Deselected: $\overline{CS}$=V_{IH}, V_{DD}=12.6V
I_{DD1}	Supply Current			75	mA	f=100KHz, V_{DD}=12.6V, Outputs Unloaded
I_{DD2}	Supply Current			90	mA	f=200KHz, V_{DD}=12.6V Outputs Unloaded

Capacitance *

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			TBD	pF	

*This parameter is periodically sampled and is not 100% tested. Condition of measurement is f=1MHz, V_{BIAS}=2V, V_{DD}=0V, and T_A=25°C.

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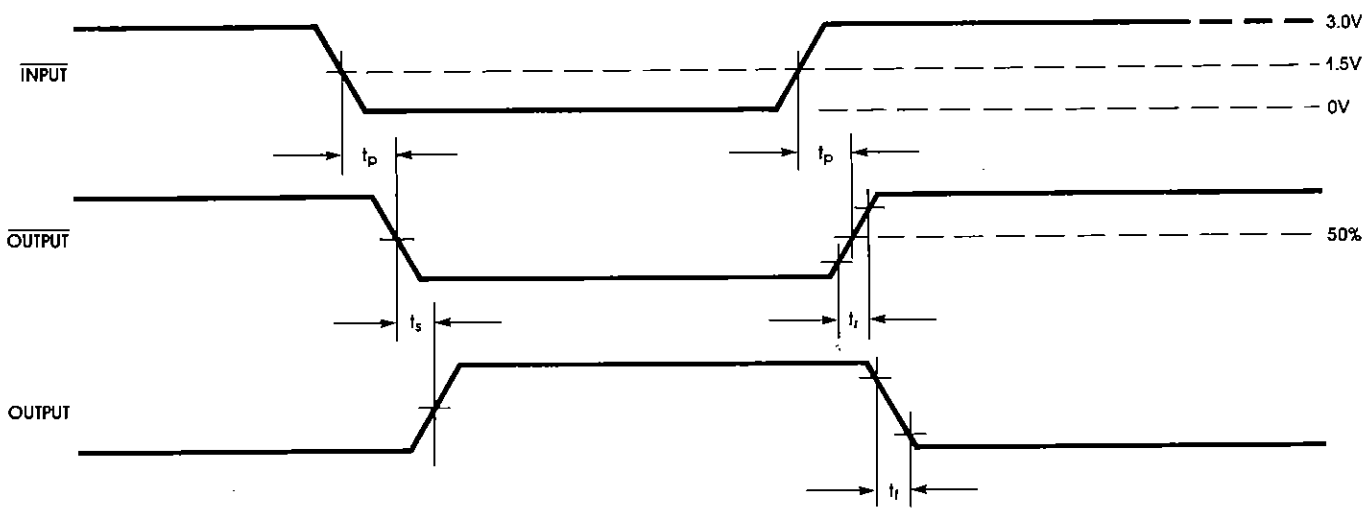
A.C. Characteristics

T_A = 0°C to 70°C, V_{DD}=12V ± 5%, unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{p1}	Propagation Delay from $\overline{X+.IN}$, $\overline{X-.IN}$, $\overline{Y+.IN}$, $\overline{Y-.IN}$			100	ns	500pF Load
t_{P2}	Propagation Delay from $\overline{CS}$ or $\overline{RESET}$			150	ns	500pF Load
t_r	Rise Time (10% to 90%)			30	ns	500pF Load
t_F	Fall Time (90% to 10%)			30	ns	500pF Load
t_S	Skew Between an Output and its Complement			15	ns	

A.C. Test Conditions



Absolute Maximum Ratings*

Ambient Temperature Under Bias ..... -20°C to +80°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin with Respect to Ground ..... -0.5 to V_{DD} + 0.5V
Supply Voltage, V_{DD} ..... -0.5 to +14V
Output Current 250mA (One Output @100% Duty Cycle)

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.